Electronic Version
Stylesheet Version v1.1.1

DIGITAL PHASE FREQUENCY DISCRIMINATOR

Abstract

A digital phase frequency discriminator has a first SR latch for generating a first output signal when set to a predetermined state, a second SR latch for generating a second output signal when set to the predetermined state, a predetermined state-detecting circuit for detecting the first and the second output signals and for outputting an RCM signal, a first predetermined state control circuit for setting the first SR latch to the predetermined state according to the RCM signal, and a second predetermined state control circuit for setting the second SR latch to the predetermined state according to the RCM signal. Both the first SR latch and the first predetermined state control circuit have a first inputting terminal for receiving a first input signal, and both the second SR latch and the second predetermined state control circuit have a second inputting terminal for receiving a second input signal.